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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,358	05/10/2004	Calvin Gabriel	US00 8015A	8246

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PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
1109 MCKAY DRIVE, M/S-41SJ
SAN JOSE, CA 95131

EXAMINER	
NGUYEN, DILINH P	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,358	GABRIEL ET AL.	
	Examiner	Art Unit	
	DiLinh Nguyen	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *1-9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group II, claims 10-20 in the reply filed on 9/1/04 is acknowledged.

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 10, 13-15, 17 and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Applicant Admitted Prior Art (fig. 1).

AAPA (fig. 1) discloses a selective etch shallow trench isolation barrier integrated circuit chip fabrication process comprising the steps of:

forming a shallow trench space in a wafer;

depositing a selective etch isolation material in a shallow trench space of a device layer 105 to form a selective etch shallow trench isolation barrier 150;

fabricating an intermetal dielectric layer 107 on top of the device layer;

etching a contact hole in the intermetal dielectric layer down to the selective etch shallow trench isolation barrier; and

filling the contact hole with conductive material 191 (fig. 1, page 3, lines 3-10).

- Regarding claims 13 and 19, AAPA discloses that the selective etch isolation material etches differently than other material adjacent to the elective selective etch isolation material (fig. 1, page 4).
- Regarding claims 14 and 20, AAPA discloses that the selective etch isolation material includes silicon nitride or oxynitride (fig. 1, page 2, lines 6-8).
- Regarding claim 15, AAPA discloses that depositing the selective etch isolation material to fill the shallow trench and removing excess elective etch isolation material by a chemical mechanical polishing (CMP) process (fig. 1, page 2, lines 6-10).
- Regarding claim 17, AAPA (fig. 1) discloses a selective etch shallow trench isolation barrier integrated circuit chip fabrication process comprising the steps of:

applying layers of oxide and nitride (fig. 1, page 2, lines 1-2);

creating a resistive mask pattern;

etching a shallow trench space;

depositing a selective etch isolation material in the shallow trench space to form a selective etch shallow trench isolation barrier;

fabricating an intermetal dielectric layer 107;

etching a contact hole in the intermetal dielectric layer down to the selective etch shallow trench isolation barrier; and

filling the contact hole with conductive material 191 (fig. 1).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11-12, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Goh et al. (U.S. Pat. 6225225).

- Regarding claims 11 and 18, AAPA (fig. 1) fails to disclose the contact hole in the intermetal layer down to the selective etch shallow trench isolation barrier is a single film layer etch step stopping on selective etch isolation material of the selective etch shallow trench isolation barrier.

Goh et al. disclose a selective etch shallow trench isolation barrier integrated circuit chip fabrication process comprising the steps of: etching the contact hole in the intermetal layer 76 down to the selective etch shallow trench isolation 56 is a single film

layer etch step stopping on selective etch isolation material of the selective etch shallow trench isolation (fig. 15, column 5, lines 55-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of AAPA to protect the silicon nitride layer overlying the trench oxide layer form the polishing step and to maintain a flat sahllow trench isolation topology (column 2, lines 50-51 and column 3, lines 1-4), as shown by Goh et al.

- Regarding claim 12, AAPA discloses that the intermetal dielectric layer compises oxide and the single film layer etch step is performed by AR, CF4, CHF3, CO and/or C4F8 (fig. 1, page 4, lines 5-8).
- Regarding claim 16, it would have been well known in the art to pre-cleaning a wafer using high purity, low particle chemicals; heating the wafer and AAPA discloses that exposing the wafer to ultra pure oxygen in a diffusion furnace under carefully controlled condition and forming a silicon dioxide film of uniform thickness of the surface of the wafer (fig. 1, page 2, lines 1-3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DLN

LONG PHAM
PRIMARY EXAMINER